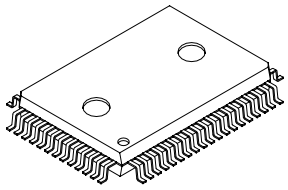
SONY

CXA2126Q

Audio/Video Switch with Electronic Volume for 2 Scart

64 pin QFP (Plastic)



Description

The CXA2126Q is an I²C programmable audio, video switch designed primarily for set top box applications. It interfaces from digital encoder sources to TV and VCR scart connectors.

Features

- 2 scart independent audio/video switching (TV, VCR)
- Compatible with 3 scart Audio/Video switch, CXA2125Q
- 0 to –63dB volume control with click noise reduction
- 3 stereo audio inputs
- I²C control
- Scart Function Switching input and output
- Scart Fast Blanking for OSD
- Mono switchable to stereo on TV and VCR outputs
- On-chip +12V to +9V voltage regulator
- Logic output
- Selectable +6dB, +12dB gain on TV output
- RGB input on VCR scart

Applications

Digital Set Top Box

Structure

Bipolar silicon monolithic IC

Absolute Maximum Ratings

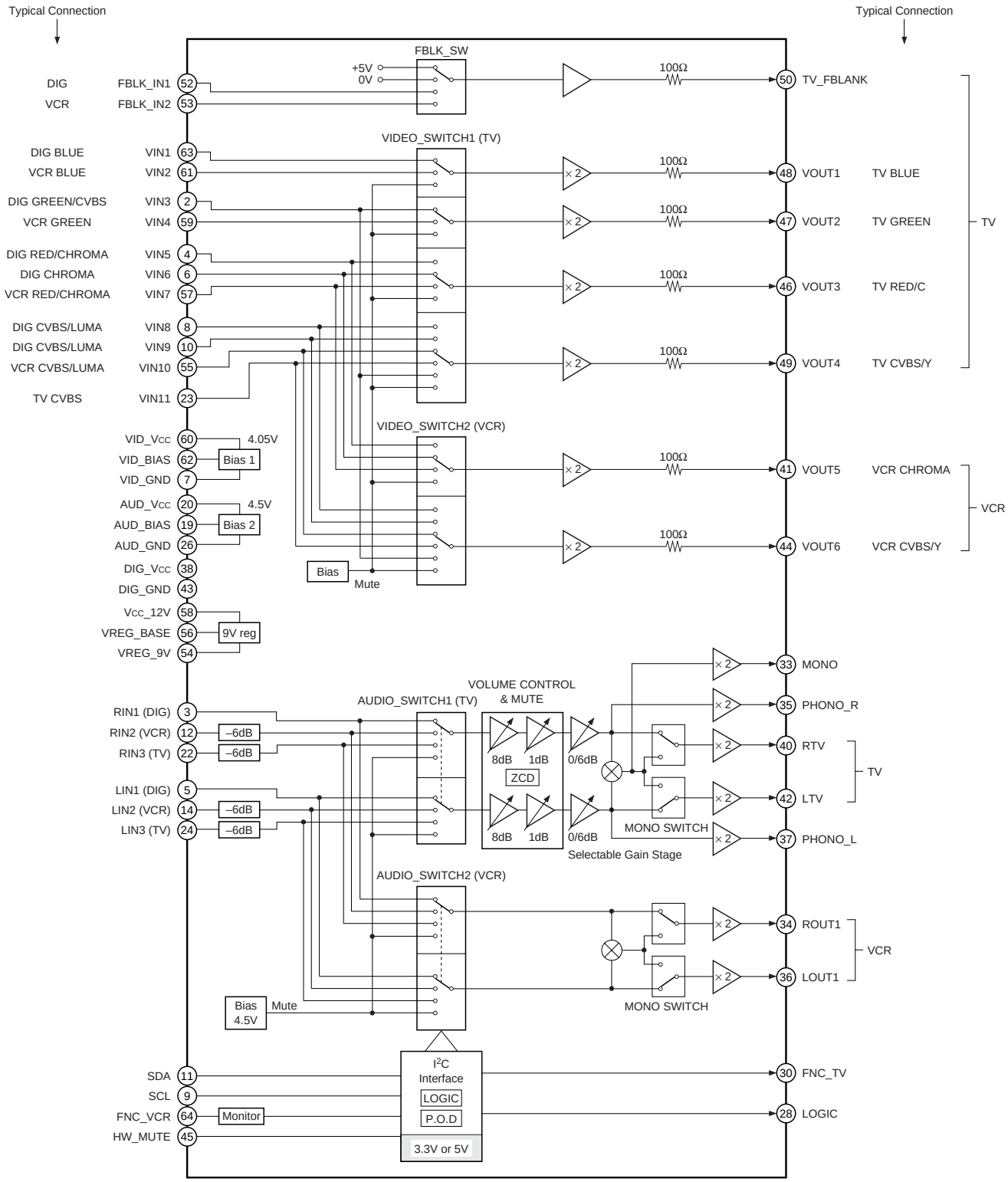
• Supply voltage	V_{CC}	12	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	850	mW

Operating Conditions

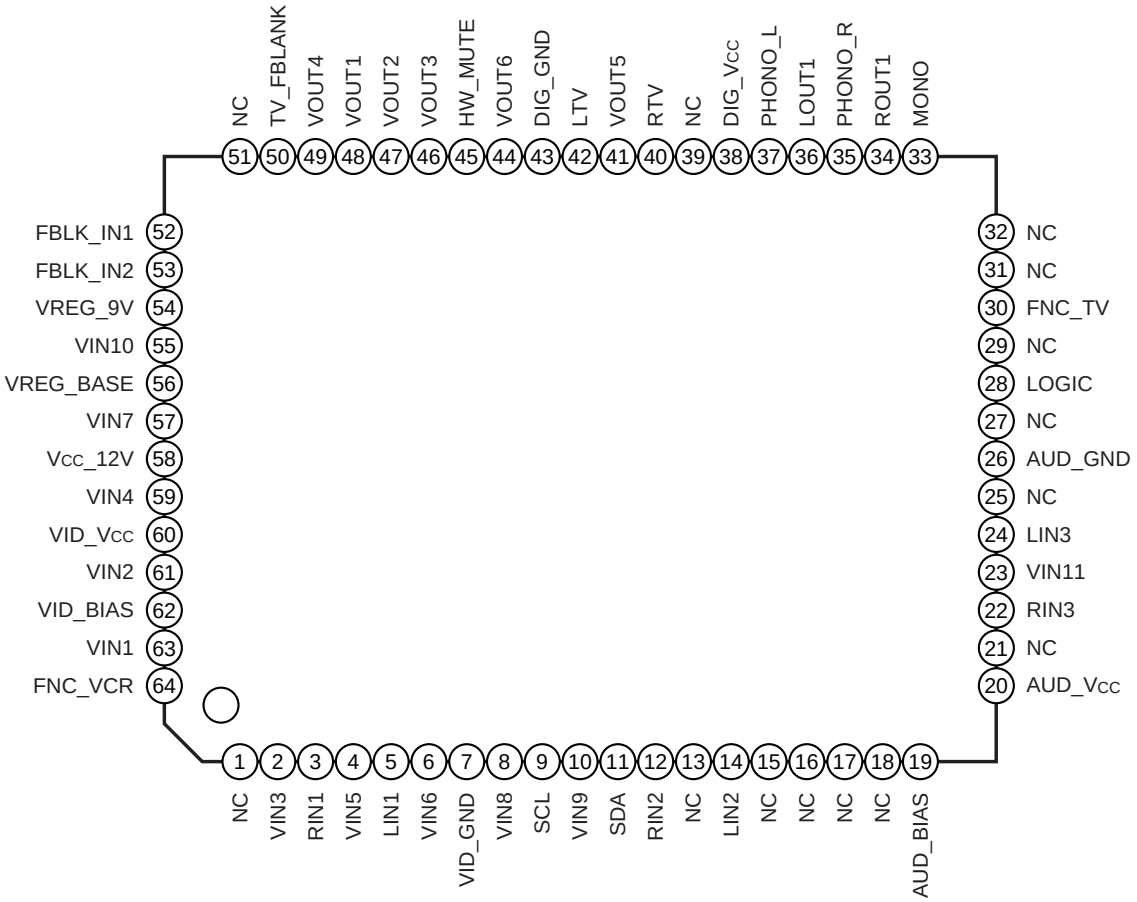
• Supply voltage	10.7 to 12	V
• Operating voltage	9 ± 0.5	V

E99339-PS

Block Diagram

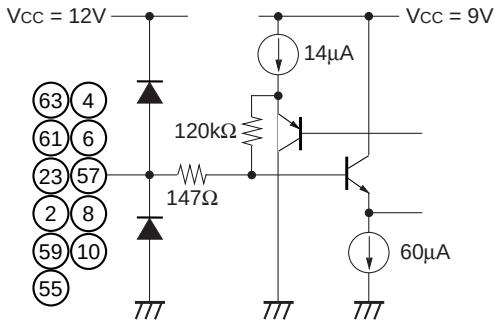
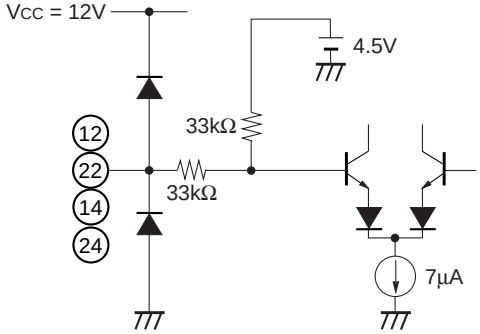
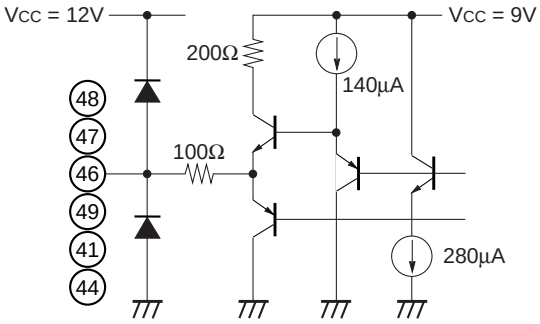
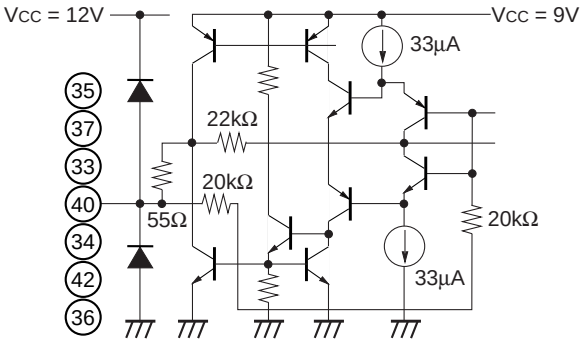


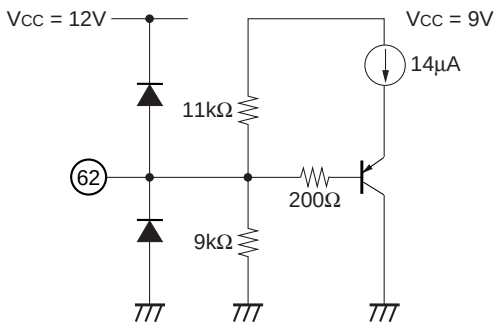
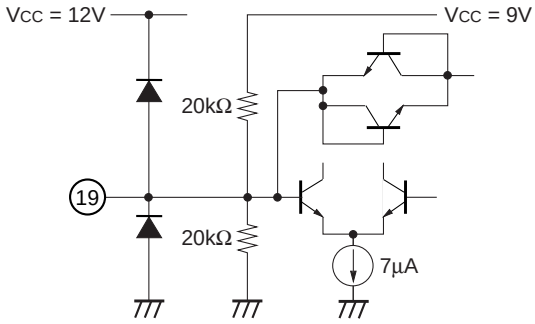
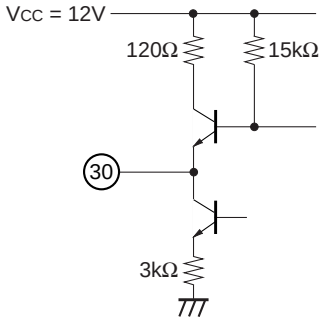
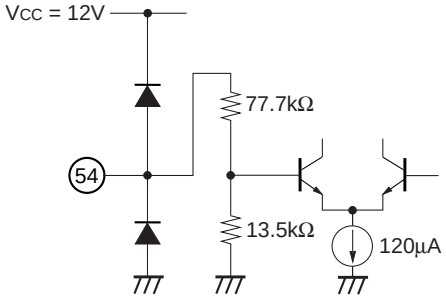
Pin Configuration

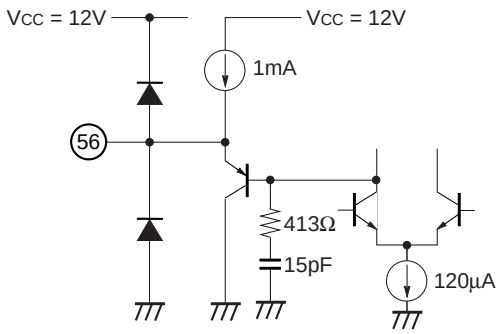
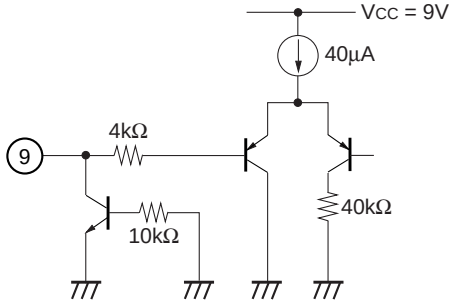
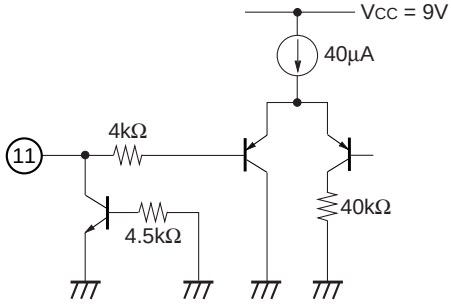
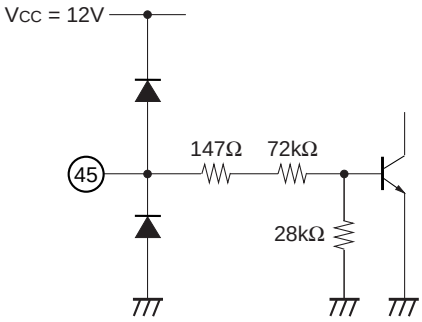


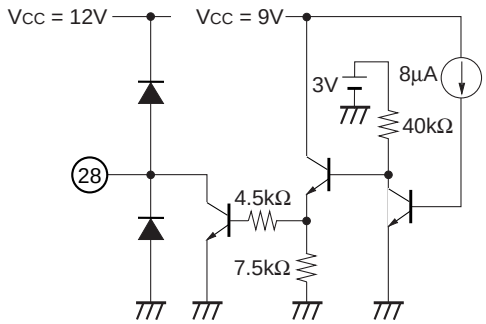
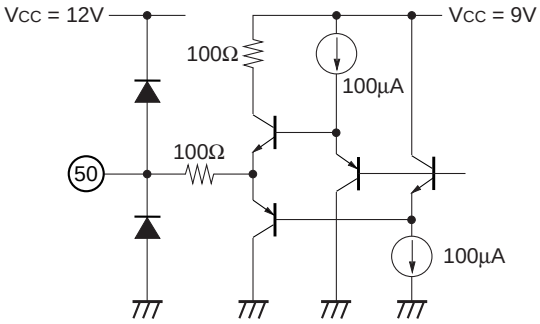
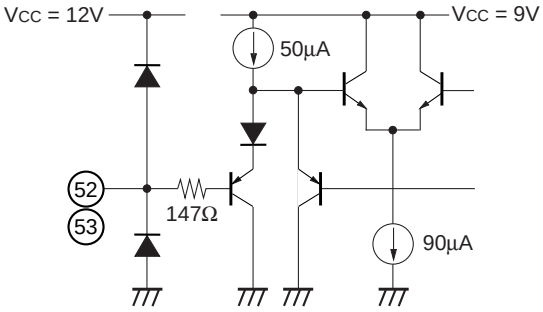
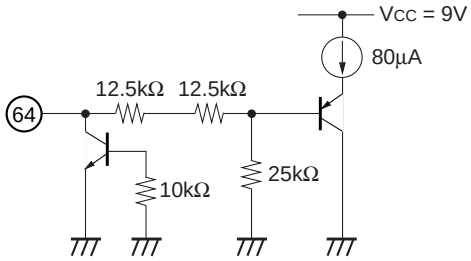
* NC = No connect

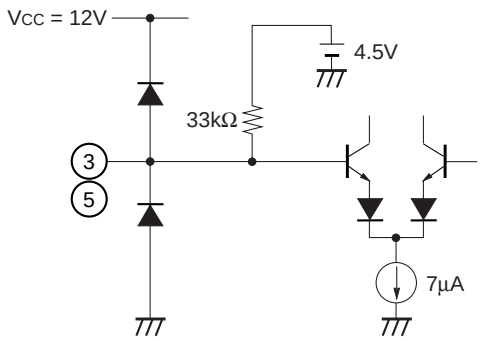
Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
63 61 2 59 4 6 57 8 10 55 23	VIN1 VIN2 VIN3 VIN4 VIN5 VIN6 VIN7 VIN8 VIN9 VIN10 VIN11	4.6V		Video signal inputs. An input coupling capacitor is required. (typ = 0.47µF)
12 22 14 24	RIN2 RIN3 LIN2 LIN3	4.5V		Audio signal inputs. An input coupling capacitor is required. (typ = 2.2µF)
48 47 46 49 41 44	VOUT1 VOUT2 VOUT3 VOUT4 VOUT5 VOUT6	3.9V		Video signal outputs.
40 34 42 36 35 37 33	RTV ROUT1 LTV LOUT1 PHONO_R PHONO_L MONO	4.5V		Audio signal outputs. A coupling capacitor may be used. (typ = 10µF)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
62	BIAS_ VIDEO	3.9V		Reference Bias for video circuit. Connected to GND with capacitor. (typ = 47µF)
19	BIAS_ AUDIO	4.5V		Reference Bias for audio circuit. Connected to GND with capacitor. (typ = 22µF)
30	FNC_TV	—		I^2C controlled output giving 0V, 6V or 12V.
54	VREG_9V	9V		Pin connected to emitter of external regulator transistor.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
56	VREG_ BASE	9.7V		Connection to base of external regulator transistor. Max I = 1mA
9	SCL	—		I^2C clock input.
11	SDA	—		I^2C data input/output.
45	HW_MUTE	—		HW MUTE: This pin is active high > 2.5V < 9V. When high, all audio outputs are muted.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
28	LOGIC	—		Open collector logic pins.
50	FBLK_ OUT	—		Fast Blank output set by I²C to input FBLK_IN1 or FBLK_IN2. High = 5.3V Low = 1.2V Connected to external emitter follower.
52 53	FBLK_IN1 FBLK_IN2	—		Fast Blank inputs. Low = < 0.4V High = > 1.0V, < 3.0V
64	FNC_VCR	—		Function switching input. (Scart pin 8)

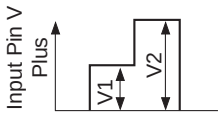
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
3 5	RIN1 LIN1	4.5V		Audio signal inputs. A coupling capacitor is required for these inputs. (typ = 2.2µF)

Electrical Characteristics

Nominal conditions (Ta = 25°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	I_{CC}	V_{CC}_12V = 12V, No signal, no load	30	50	80	mA

Video system Nominal conditions (Ta = 25°C, Vcc_12V = 12V, VREG_9V = 9V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input pin voltage	V_{VPin}	No signal, no load (Fig.1)	4.3	4.6	4.9	V
Output pin voltage – with output on.	V_{VPout1}	No signal, no load (Fig.1)	3.6	3.9	4.2	V
Output pin voltage – with output off.	V_{VPout2}	No signal, no load (Fig.1)	—	0	0.5	V
Gain	GVv	f = 200kHz, 0.3Vp-p input (Fig.2)	5.5	6.0	6.5	dB
Bandwidth	f_{V3dB}	0.3Vp-p input, frequency where output level is –3dB with 200kHz serving as 0dB (Fig. 2)	15	20	—	MHz
Input dynamic range	V_{DRVI}	200kHz input (Fig.2)	2.5	—	—	Vp-p
Output dynamic range	V_{DRVO}	200kHz, 2.5Vp-p input (Fig.2)	5.0	—	—	Vp-p
Cross talk	Vctv	f = 4.43MHz, 1Vp-p input (Fig.2)	—	—	–50	dB
S/N ratio	S/N_V	Ratio of 0.7Vp-p white video signal to "black line" noise. Weighted using CCIR 567. HPF @5kHz, LPF @5MHz. (Fig.2)	—	72	—	dB
Input impedance	Zin_V	1Vrms 1kHz input through 56kΩ. Attenuation measured to calculate Zin_V (Fig.3)	80	120	175	kΩ
Non-linearity	Lin	 (Fig.4) V1 = Pin voltage +0.5V, V2 = Pin voltage +1V At output, non-linearity = $\left(\frac{V2}{V1 \times 2} - 1\right) \times 100$	–3	–0.4	3	%
Differential gain	DG	1.7Vp-p 5-step modulated staircase. (Chroma and Burst are 150mVp-p 4.43MHz) (Fig.2)	–3	1.5	2	%
Differential phase	DP	as above. (Fig.2)	–3	1	2	Deg
Sync crush	SC	Percentage reduction in sync pulse (0.4Vp-p), with tip at –1.2V input offset. (Fig.4)	–2	0	2	%

Audio system

Unless otherwise stated: input coupling capacitor 1µF; output coupling capacitor of 10µF; load of 10kΩ.

Nominal conditions (Ta = 25°C, Vcc_12V = 12V, VREG_9V = 9V)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit
Input/output pin voltage		V_{APIN}	No signal, no load (Fig. 5)	4.2	4.5	4.8	V
Gain Input	Output						
RIN1/LIN1	TV/Phono	GV_{A1}	f = 1kHz, 0.5Vrms input. TV output amplifier set to 0dB (Fig. 6)	5.5	6	6.5	dB
RIN1/LIN1	TV/Phono	GV_{A2}	f = 1kHz, 0.5Vrms input. TV output amplifier set to +6dB (Fig. 6)	11	12	13	dB
RIN1/LIN1	VCR	GV_{A3}	f = 1kHz, 1Vrms input. (Fig. 6)	—	6	—	dB
RIN1 + LIN1	TV mono	GV_{A4}	f = 1kHz, 0.5Vrms stereo input. TV output amplifier set to 0dB (Fig. 6)	—	6	—	dB
RIN1 + LIN1	TV mono	GV_{A5}	f = 1kHz, 0.5Vrms stereo input. TV output amplifier set to +6dB (Fig. 6)	—	12	—	dB
RIN1 + LIN1	VCR mono	GV_{A6}	f = 1kHz, 0.5Vrms stereo input. (Fig. 6)	—	6	—	dB
RIN2, 3 LIN2, 3	TV/Phono	GV_{A7}	f = 1kHz, 1Vrms input. TV output amplifier set to 0dB (Fig. 6)	–0.5	0	+0.5	dB
RIN2, 3 LIN2, 3	TV/Phono	GV_{A8}	f = 1kHz, 1Vrms input. TV output amplifier set to +6dB (Fig. 6)	5.5	6	6.5	dB
RIN2, 3 + LIN2, 3	TV mono	GV_{A9}	f = 1kHz, 1Vrms stereo input. TV output amplifier set to 0dB (Fig. 6)	–0.7	0	+0.3	dB
RIN2, 3 + LIN2, 3	TV mono	GV_{A10}	f = 1kHz, 1Vrms stereo input. TV output amplifier set to +6dB (Fig. 6)	5	6	7	dB
RIN2, 3 LIN2, 3	VCR	GV_{A11}	f = 1kHz, 1Vrms input. (Fig. 6)	–0.5	0	+0.5	dB
RIN2, 3 + LIN2, 3	VCR mono	GV_{A12}	f = 1kHz, 1Vrms stereo input. (Fig. 6)	–0.7	0	+0.3	dB
Audio frequency response		F_{AF}	0.3Vp-p input. Output level at 30kHz with 1kHz serving as 0dB. (Fig. 7)	–0.3	0	+0.3	dB
Frequency B/W		F_{BWA1}	0.3Vp-p input; frequency where output level is –3dB with 1kHz serving as 0dB. No load (Fig. 7)	—	1	—	MHz
Distortion		THD	f = 1kHz, 0.5Vrms, unweighted response; LPF @400Hz, HPF @80kHz. (Fig. 6)	—	0.003	0.2	%
Input dynamic range RIN2, 3 LIN2, 3		V_{dA1}	f = 1kHz (Fig. 6)	2	—	—	Vrms
Input dynamic range RIN1, LIN1		V_{dA2}	f = 1kHz (Fig. 6)	1	—	—	Vrms
Cross talk (Switch separation)		V_{ctA}	f = 1kHz, 1Vrms input on one input, measure on any other audio output. (Fig.6)	—	—	–76	dB

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
DC offset	Voff	Offset voltage between input and output (Fig. 5)	–30	—	+30	mV
Input impedance RIN2, 3/LIN2, 3	Zin1	(excluding any external series resistor)	—	66	—	kΩ
Input impedance RIN1/LIN1	Zin2	(excluding any external series resistor)	—	33	—	kΩ
Output impedance	Zout	(excluding any external series resistor)	—	10	—	Ω
Phase difference	Vpda	f = 1kHz, 1Vrms input to two channels. Phase difference of stereo output measured	—	0.05	—	Deg
S/N ratio	S/N_A	f = 1kHz, 1Vrms input (at maximum volume). HPF @20Hz, LPF@20kHz. (Fig. 6)	80	90	—	dB
Electronic Volume Control						
Fine volume attenuation step	A_{EVC}	f = 1kHz, 0.5Vrms input. Set by I^2C. (Fig.6)	0.6	1	1.4	dB
Coarse volume attenuation step	A_{EVF}	f = 1kHz, 0.5Vrms input. Set by I^2C. (Fig.6)	7.5	8	8.5	dB
Mute	Amute	f = 1kHz, 1Vrms input. (Fig.6)	—	—	–80	dB
DC Offset -RTV, LTV	VoffTV	Offset voltage between any audio input and RTV, LTV outputs. (Fig.5)	–30	0	+30	mV

I²C Electrical Characteristics

Nominal conditions (Ta = 25°C, Vcc_12V = 12V, VREG_9V = 9V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}		2.3	—	5.0	V
Low level input voltage	V_{IL}		0	—	1.5	V
Low level output voltage	V_{OL}	With SDA, 3mA current supplied	0	—	0.4	V
Maximum clock frequency	f_{SCL}		0	—	100	kHz
Minimum waiting time for data change	t_{BUF}		4.5	—	—	µs
Minimum waiting time for data transfer start	$t_{HD;STA}$		4.0	—	—	µs
Low level clock pulse width	t_{LOW}		4.7	—	—	µs
High level clock pulse width	t_{HIGH}		4.0	—	—	µs
Minimum waiting time for start preparation	$t_{SU;STA}$		4.7	—	—	µs
Minimum data hold time	$t_{HD;DAT}$		5	—	—	s
Minimum data preparation time	$t_{SU;DAT}$		250	—	—	ns
Rise time	t_R		—	—	1	µs
Fall time	t_F		—	—	300	ns
Minimum waiting time for stop preparation	$t_{SU;STO}$		4.7	—	—	µs

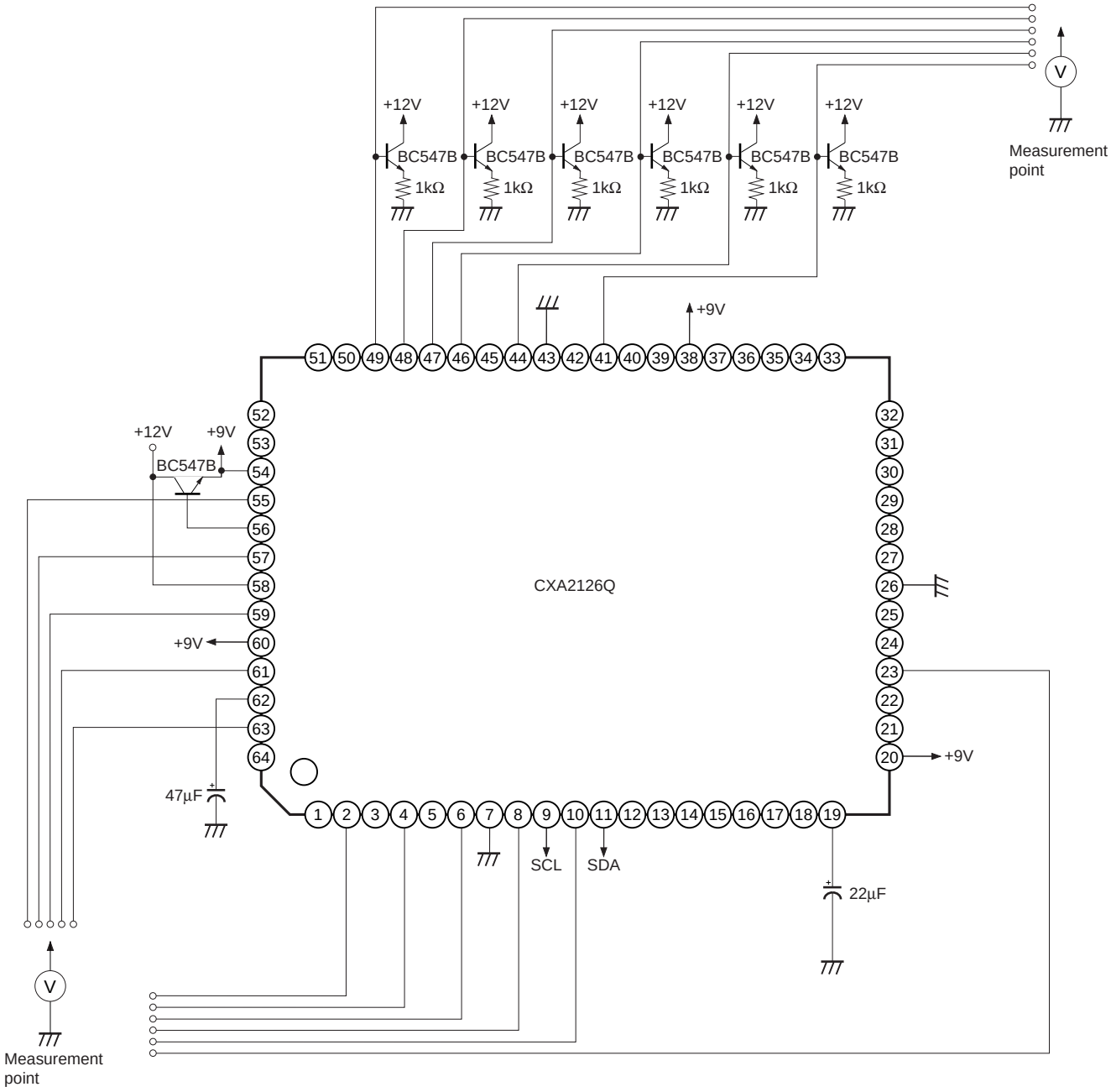


Fig. 1. Video system (d.c. test)

Signal applied to Pins 2, 4, 6, 8, 10, 23, 55, 57, 59, 61, 63
Output signal measured from Pins 41, 44, 46, 47, 48, 49

Notes) 1. All +9V supplies de-coupled close to supply pins, 20, 38, 60 with 10nF ceramic capacitor.
2. All video outputs are loaded with emitter follower during tests.

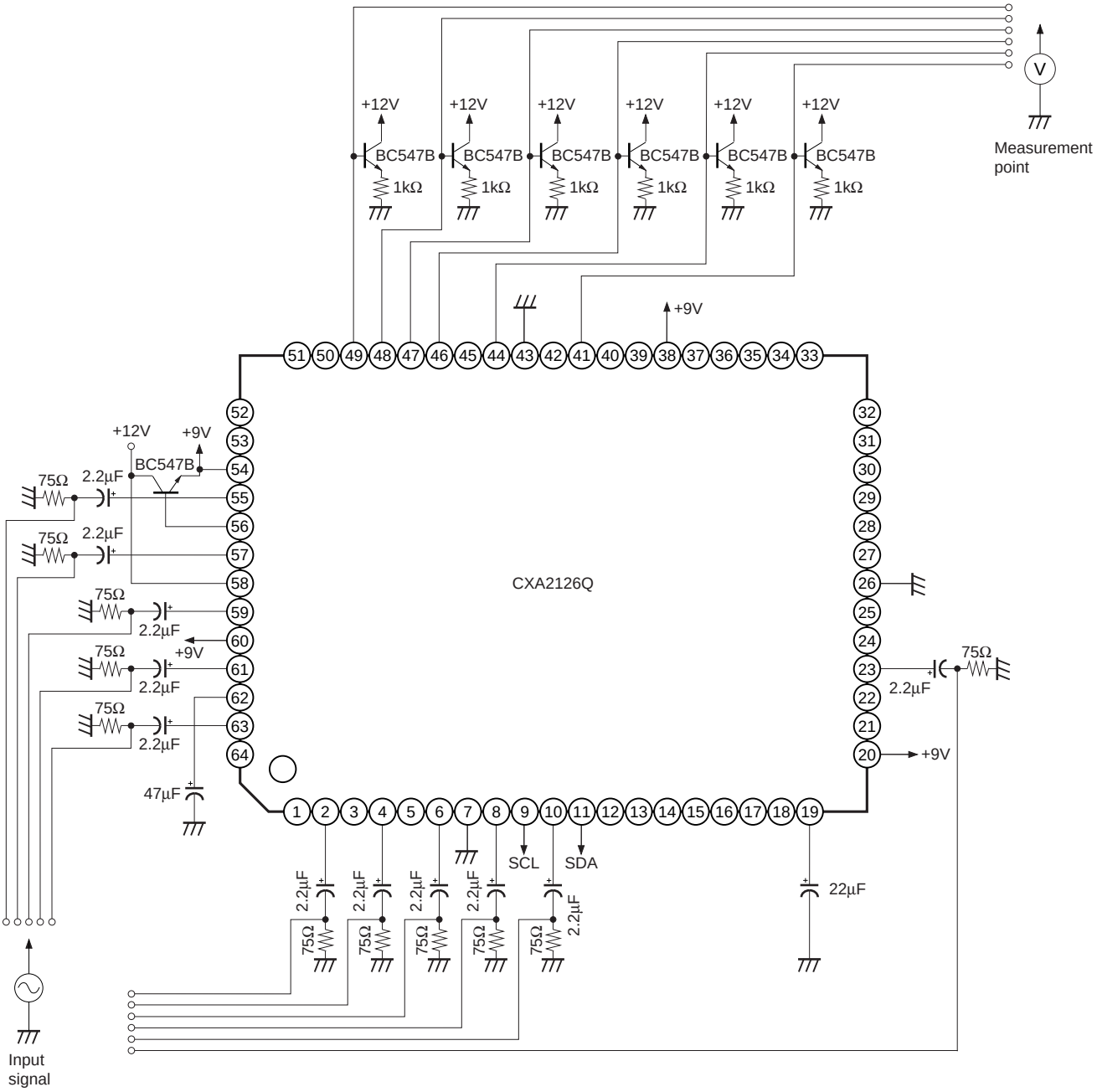


Fig. 2. Video system (gain, dynamic range, bandwidth, differential gain, differential phase, crosstalk, signal to noise)

Signal applied to Pins 2, 4, 6, 8, 10, 23, 55, 57, 59, 61, 63
Output signal measured from Pins 41, 44, 46, 47, 48, 49

Notes) 1. All +9V supplies de-coupled close to supply pins, 20, 38, 60 with 10nF ceramic capacitor.
2. For tests requiring video measuring equipment with 75Ω input impedance, an external video line driver or buffer is used.
3. All video outputs are loaded with emitter follower during tests.

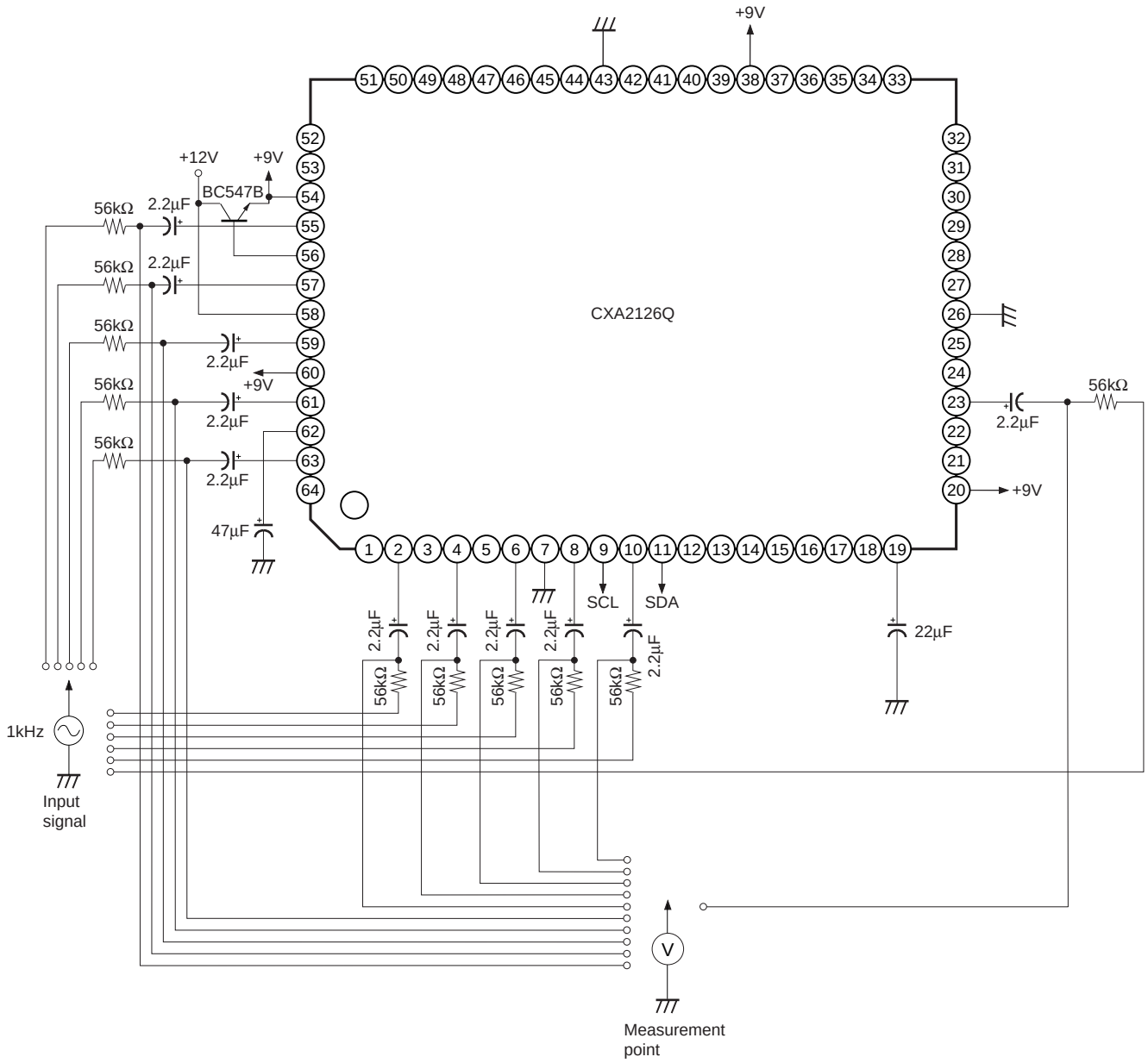


Fig. 3. Video system (input impedance)

Signal applied and measured from Pins 2, 4, 6, 8, 10, 23, 25, 55, 57, 59, 61, 63

Notes) 1. All +9V supplies de-coupled close to supply pins, 20, 38, 60 with 10nF ceramic capacitor.
2. Voltage measurements carried out with a high input impedance DVM. Typically 10GΩ.

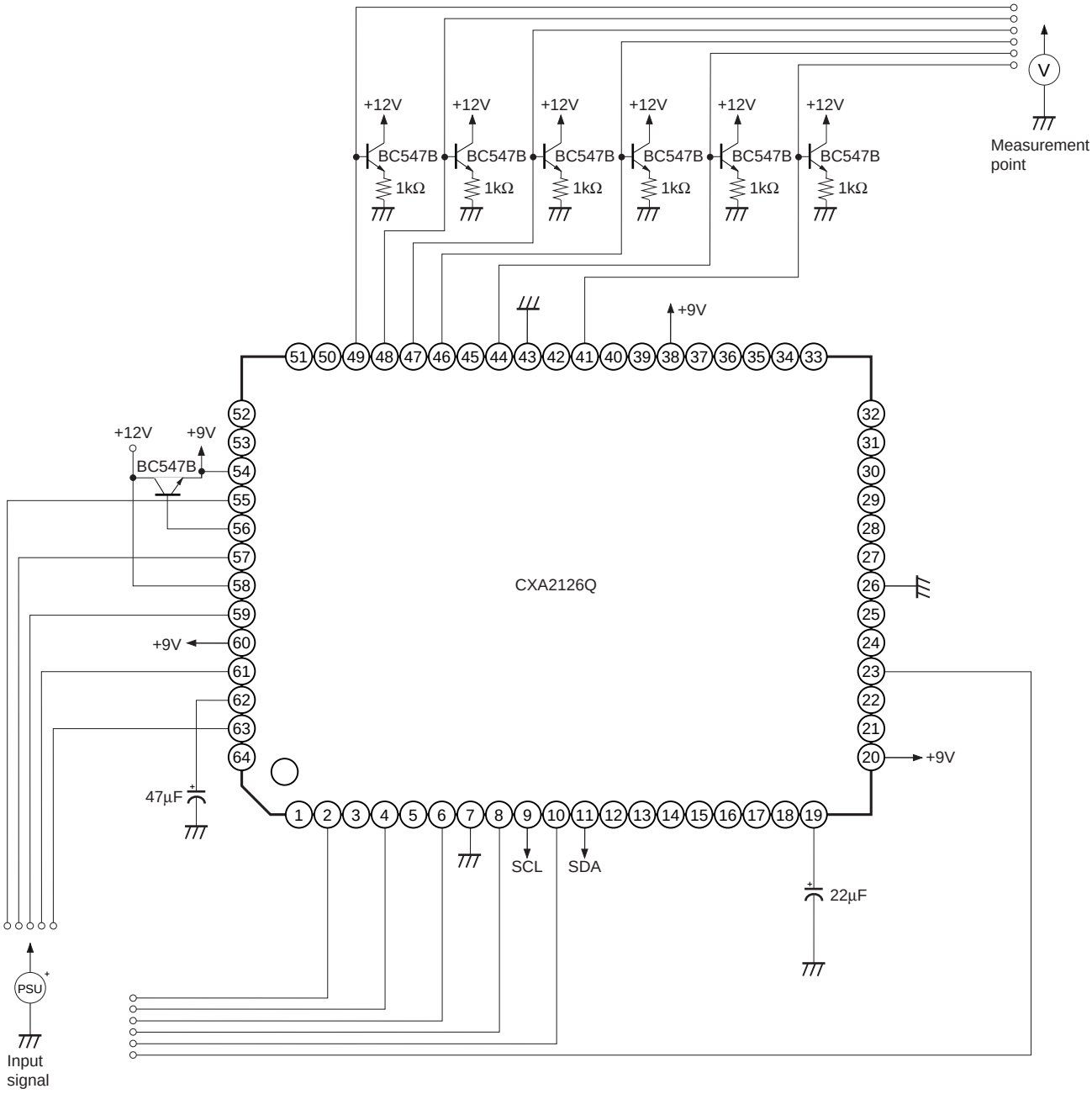


Fig. 4. Video system (linearity)

Signal applied to Pins 2, 4, 6, 8, 10, 23, 55, 57, 59, 61, 63
Output signal measured from Pins 41, 44, 46, 47, 48, 49

Notes) 1. All +9V supplies de-coupled close to supply pins, 20, 38, 60 with 10nF ceramic capacitor.
2. All video outputs are loaded with emitter follower during tests.

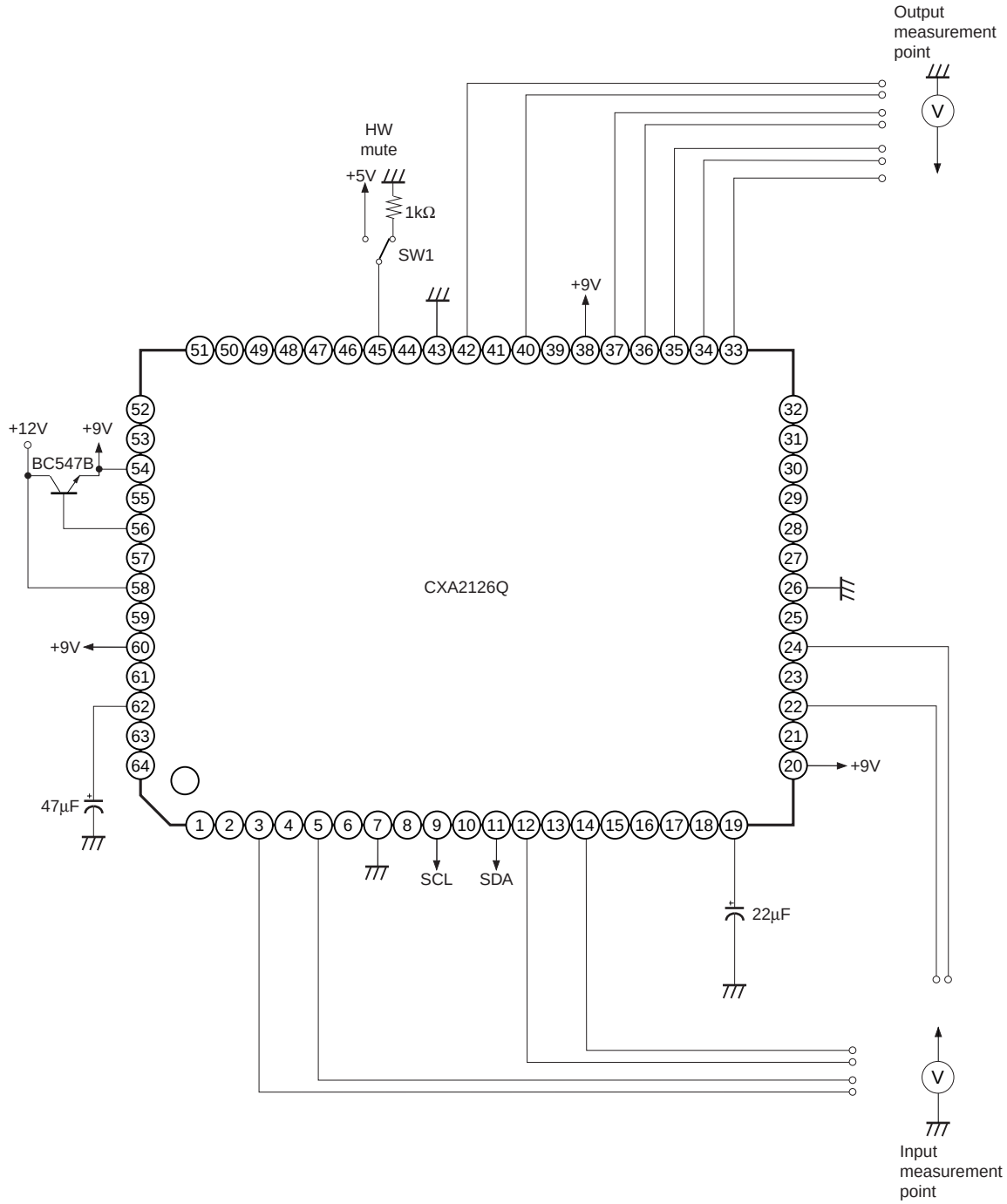


Fig. 5. Audio system (d.c. tests)

d.c. measured from pins: 3, 5, 12, 14, 22, 24, 33, 34, 35, 36, 37, 40, 42

Note) All +9V supplies de-coupled close to supply pins, 20, 38, 60 with 10nF ceramic capacitor.

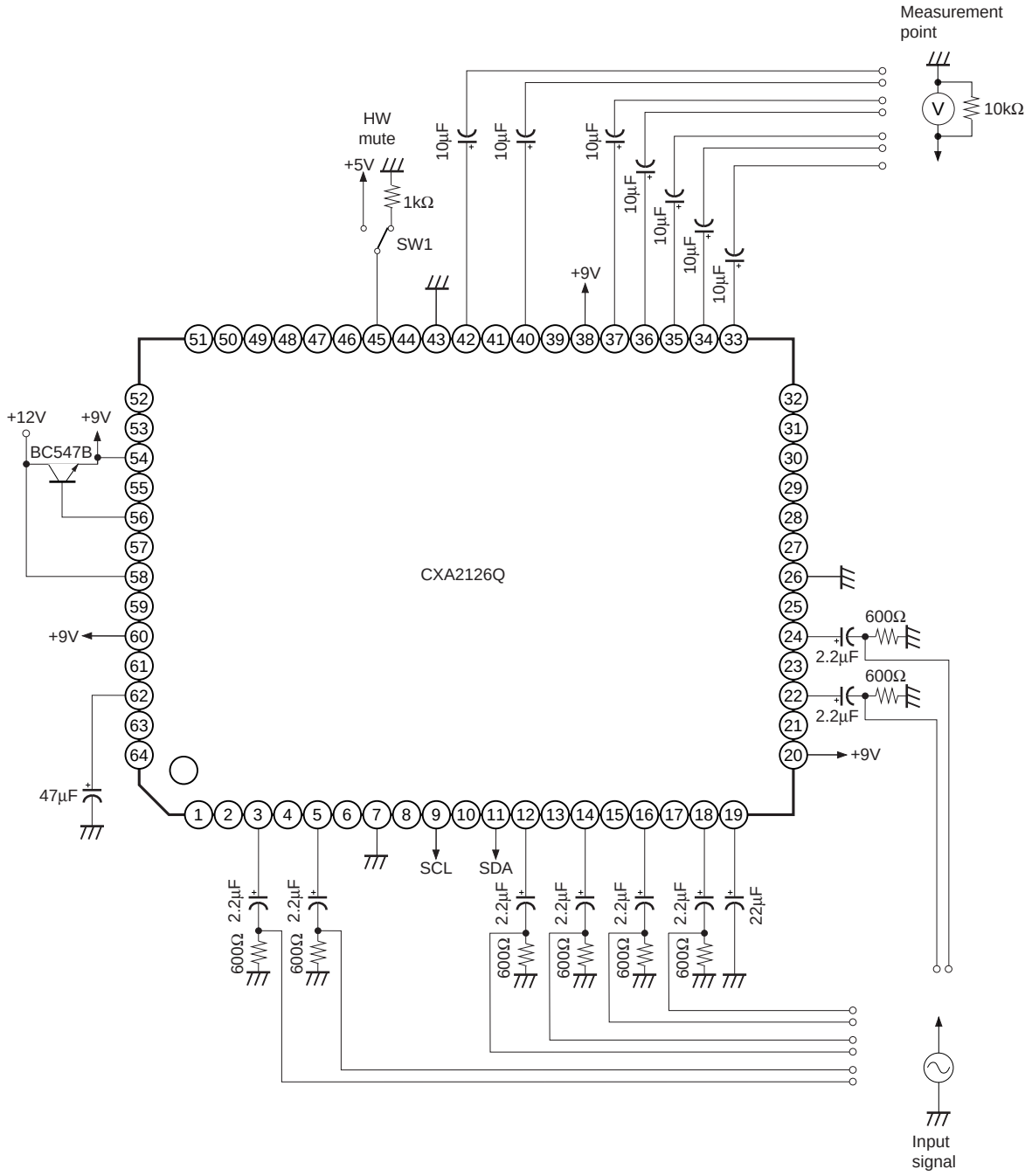


Fig. 6. Audio system (gain, dynamic range, signal to noise, crosstalk, distortion, volume control)

Signal applied to Pins, 3, 5, 12, 14, 22, 24
Output signal measured from Pins 33, 34, 35, 36, 37, 40, 42

Notes) 1. All +9V supplies de-coupled close to supply pins, 20, 38, 60 with 10nF ceramic capacitor.
2. When muting audio using hardware mute, SW1 is closed.

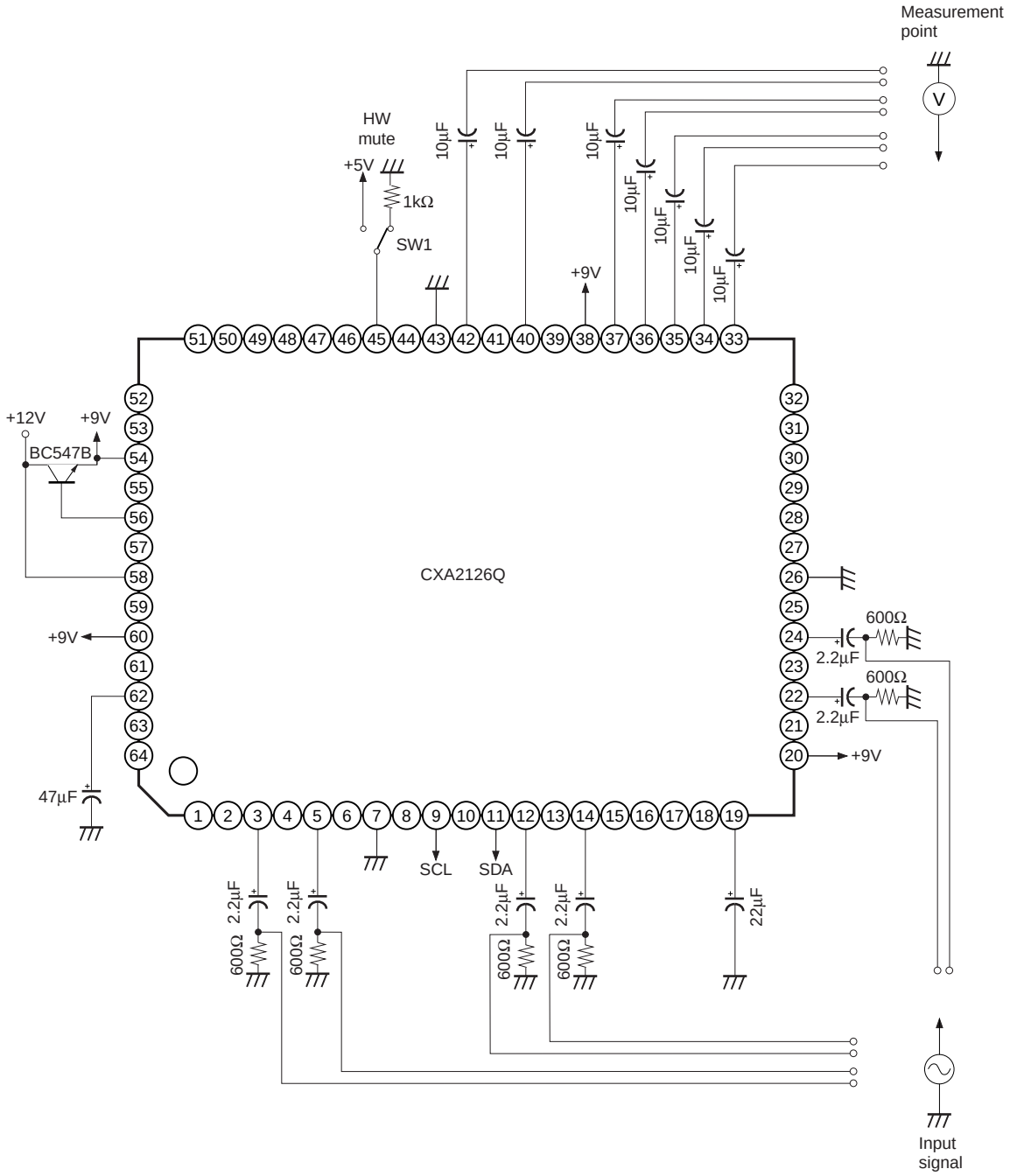
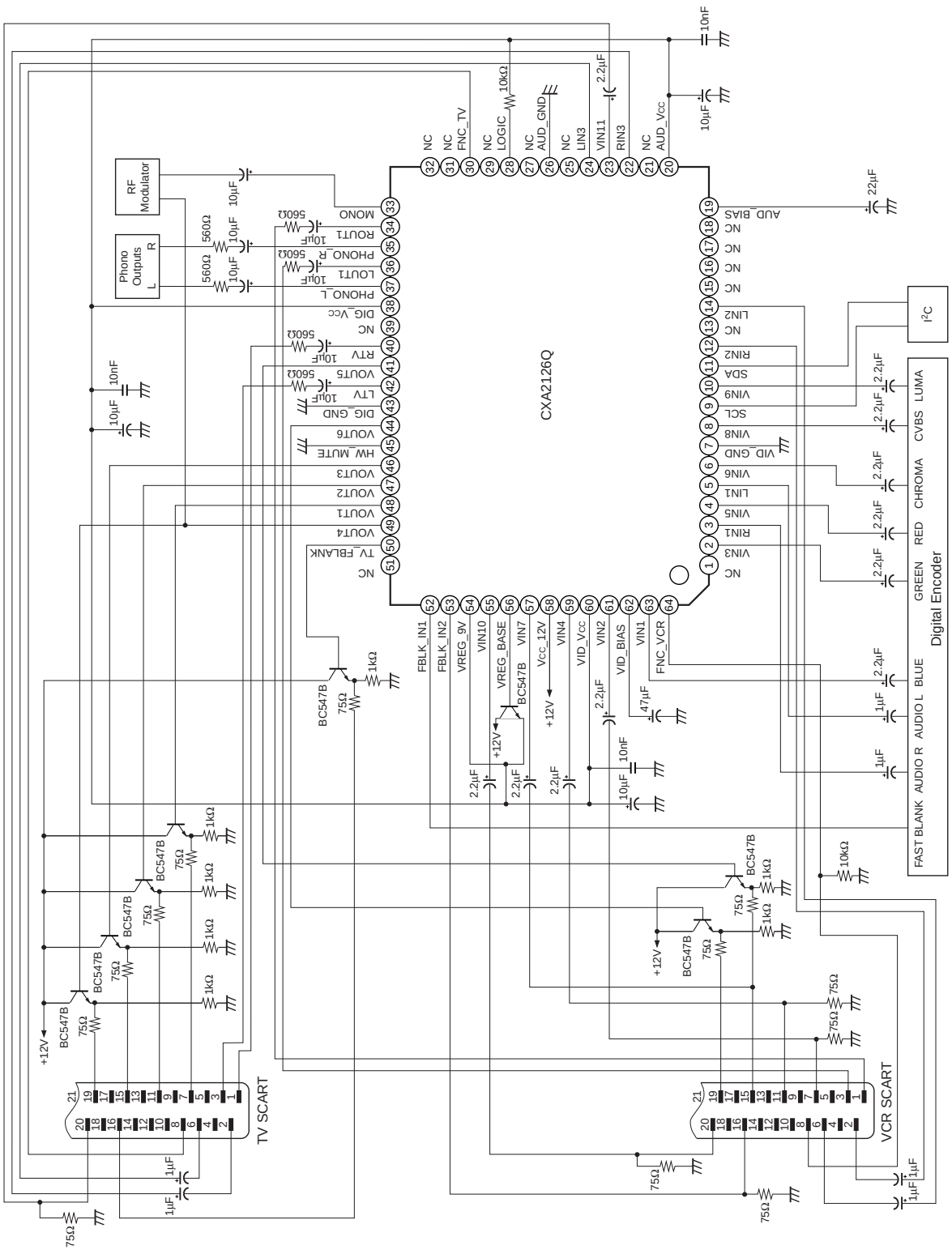


Fig. 7. Audio system (bandwidth and frequency responce)

Signal applied to Pins, 3, 5, 12, 14, 22, 24
Output signal measured from Pins 33, 34, 35, 36, 37, 40, 42

Notes) 1. All +9V supplies de-coupled close to supply pins, 20, 38, 60 with 10nF ceramic capacitor.
2. When muting audio using hardware mute, SW1 is closed.

Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

1. Explanation of Video Section

The video section comprises of 11 high impedance inputs switched through to 6 video outputs. A +6dB internal amplifier is connected to each output. The amplifier is required to compensate for the 6dB attenuation which occurs at the external emitter follower stage used for driving video loads. All video outputs have an integrated 100Ω series protection resistor. The typical external configuration is shown in Fig. 1-1.

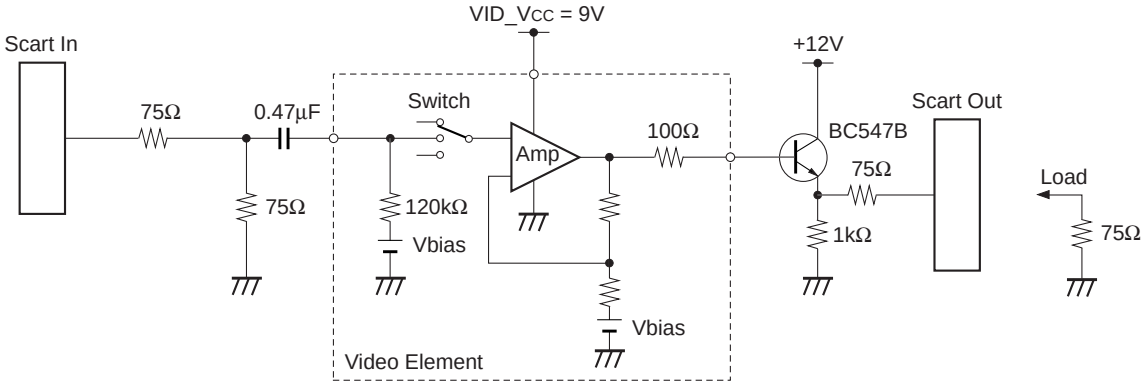


Fig. 1-1. Video Circuit Element: 6dB gain amplifier with external emitter follower

Switching the Video Outputs Off

Each video output can be individually turned off using the I^2C. When turned off, the output is high impedance and hence the current consumption of the external emitter followers is reduced.

2. Explanation of Audio System

Inputs and Outputs

The audio system consists of 3 stereo inputs, 2 stereo outputs and separate mono and phono outputs. The stereo outputs can be connected to any one of the 3 stereo inputs. All audio inputs have a –6dB attenuator except RIN1 and LIN1. Thus, the net gain of the audio system is 0dB, as the internal switch is followed by an audio amplifier having +6dB of gain. The stereo input RIN1/LIN1 does not have an input attenuator and therefore the net gain from input to output is +6dB. The output impedance of each audio amplifier is near zero, and can be capacitively coupled directly to the external scart circuit. The output circuitry is typically a 10µF capacitor, and an optional 560Ω series compliance resistor. Depending on the length and type of cable used in the scart cable connector, the load seen at the scart terminal will consist of a parallel capacitor, (100pF to 400pF) and mandatory 10kΩ resistor connected to ground. The customer may chose to place an alternative audio filter at the AV switch output.

TV Audio Output

The TV audio section is composed of an audio switch followed by two variable gain stages, corresponding to the coarse and fine electronic volume control. The coarse volume control gives a 0 to –56dB range in 8dB steps. Similarly the fine control gives a 0 to –7dB range in 1dB steps. The volume control section is followed by a switchable 0/+6dB amplifier which allows compensation for low level signals from a DAC. Finally, a mono switch allows the mixed R + L signal to be switched to the R and L output channels. (Fig. 2-1)

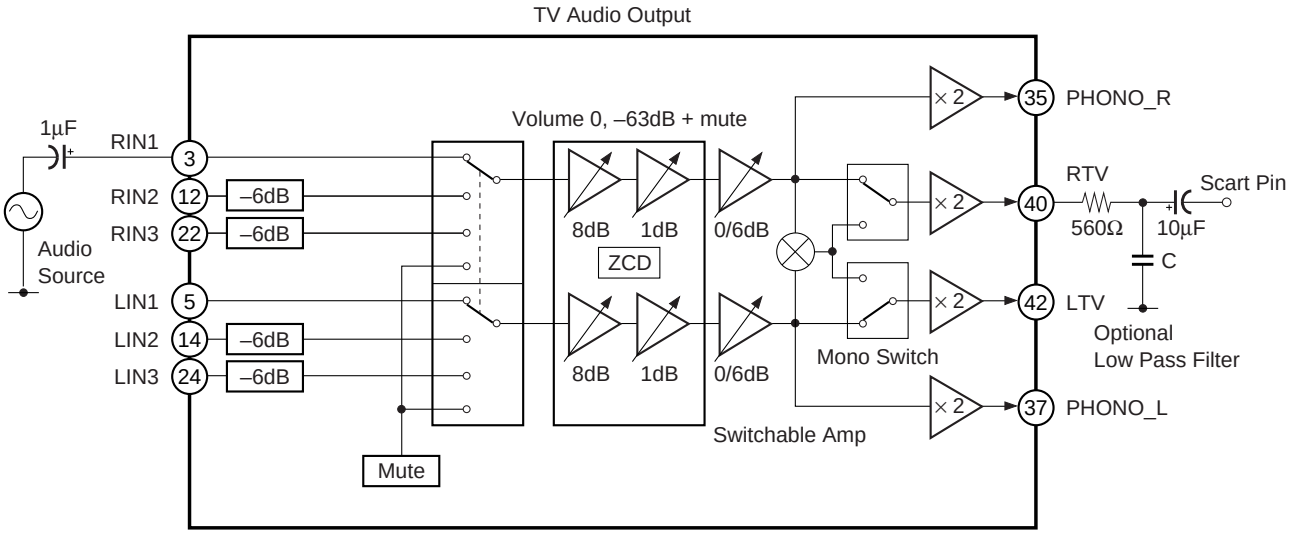


Fig. 2-1. TV Audio Output

TV Mute

The I^2C mute function acts only on the TV, phono and mono audio circuit. Audio mute can be implemented after a audio zero cross detection to reduce click noise, or immediately depending on the I^2C setting of ZCD. It can be seen from the I^2C write format that the same mute bit occurs in DATA 1 and DATA 7. This allows the software to action an immediate mute, make any suitable changes to the audio source or electronic volume control and after a minimum period of 6 × 90µs (540µs) un-mute the output buffer. Such a period provides ample time to allow any transient ac voltages to settle during an audio source change.

Zero Cross Detector (ZCD)

The zero cross detector reduces the effect of "click noise" when implementing a volume change or an audio mute. The change volume or mute instruction sent by I^2C will only be implemented when a minimal (ie zero cross) signal amplitude is detected.

The zero cross detection circuit can be turned off by setting the "ZCD" bit low in the I^2C write mode.

Hardware Mute

A hardware mute pin is provided which will mute all audio outputs when the pin voltage exceeds 2.5V. This muting is instantaneous.

VCR Output

The outputs ROUT1 and LOUT1 have a fixed gain of 0dB from the input. If any attenuation is required then it is possible to insert a series resistance on the input. (Fig. 2-2)

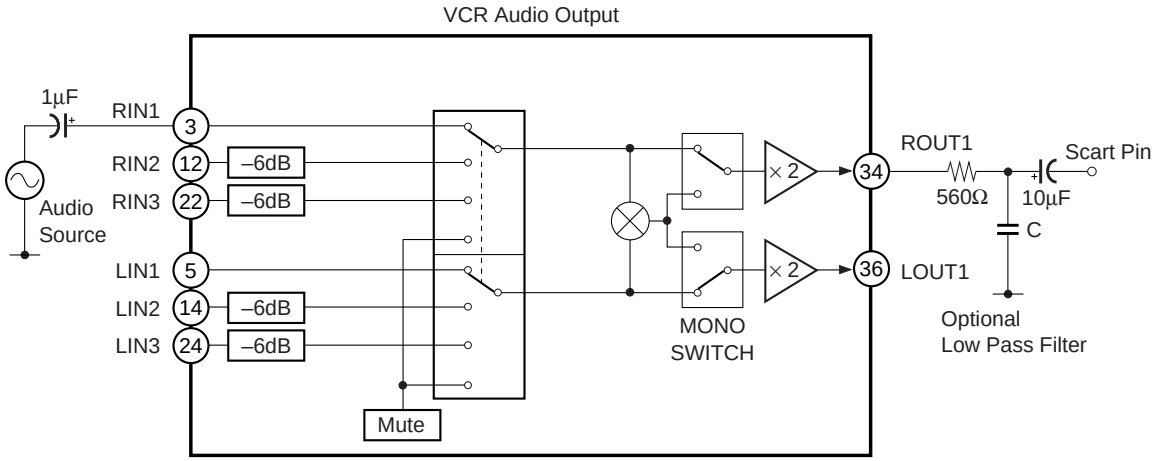


Fig. 2-2. VCR Audio Output

Phono Outputs

There is a stereo phono output which carries the same signal as the TV output. This is typically used for connection to a hi-fi. The user may connect an external attenuator which is a.c. coupled to the outputs.

Mono Output

The mono output is a mix of the TV right and left channels.

I²C Data Interface Table

IC Control Data Format

S	Slave address	A	DATA1	A	DATA2	A	DATA3	A	DATA4	A	DATAn	A	P

S: Start condition A: Acknowledge P: Stop condition

Address = 90H

I²C Data Structure (write mode)

	b7	b6	b5	b4	b3	b2	b1	b0
Address	1	0	0	1	0	0	0	0 = Write
Data1	EVC			EVF			TV Aud Mute	Z.C.D
Data2	Not used	Not used	Vid_Switch 1 TV			Aud_Switch 1 TV		
Data3	Vout5 Mute	Not used	Vid_Switch 2 VCR			Aud_Switch 2 VCR		
Data4	Not used	Not used	Not used			Not used		
Data5	Not used	Not used	FBLK			FNC		LOGIC
Data6	Not used	Not used	Vout6 on/off	Vout5 on/off	Vout4 on/off	Vout3 on/off	Vout2 on/off	Vout1 on/off
Data7	TV Aud Mute	TV Aud Gain	Not used	mono VCR	mono TV	Not used	Not used	Not used

Key

EVC: Electronic Volume Course (8dB steps)
EVF: Electronic Volume Fine (1dB steps)
TV Aud Mute: TV Audio mute. Controls the TV audio output buffer. (Same bit appears in data 1 & 7)
Z.C.D: Zero cross detector active. When ZCD = 1 volume and mute change at zero cross.
Vid_Switch 1: Selects the input video sources for Vout1, Vout2, Vout3, Vout4
Vid_Switch 2: Selects the input video sources for Vout5, Vout6
Aud_Switch 1: Selects one of 3 stereo inputs for RTV, LTV. PHONO_L, PHONO_R, MONO
Aud_Switch 2: Selects one of 3 stereo inputs for Rout1, Lout1
FNC: Video function switch control
FBLK: Video Fast Blanking control
LOGIC: Logic outputs (open collector). 0 = high impedance. 1 = current sink mode.

I²C Data Format (read mode)

S	Slave address	A	DATA8	NA	P

NA: No Acknowledge

I²C Data Structure (read mode)

	b7	b6	b5	b4	b3	b2	b1	b0
Address	1	0	0	1	0	0	0	1 = Read
Data	x	x	ZC Status	P.O.D.	x		FNC_VCR	

Key

FNC_VCR: At Pin 64, AV switch monitors the voltage of pin 8 from VCR scart, and records status.

ZC Status: ZC Status = 1 indicates that zero cross condition has been achieved after the ZCD is turned on.

P.O.D.: Power On Detect. P.O.D. = 1 when DIG_V_{CC} voltage rises above a threshold level of approximately 5V.

3. Video Input I²C Control

Switch 1 (TV Output) Data 2 Bits 3, 4, 5

Switch setting	Vout1 (B)	Vout2 (Green)	Vout3 (R/C)	Vout4 (CVBS/Y)	Comment
0 x x 0 0 0 x x x	VIN1	VIN3	VIN5	VIN8	Digital encoder
1 x x 0 0 1 x x x	Bias	Bias	VIN6	VIN9	Digital encoder
2 x x 0 1 0 x x x	VIN2	VIN4	VIN7	VIN10	VCR
3 x x 0 1 1 x x x	Not used	Not used	Not used	Not used	Not used
4 x x 1 0 0 x x x	Bias	Bias	VIN5	VIN3	Digital encoder
5 x x 1 0 1 x x x	Bias	Bias	Bias	VIN11	TV
6 x x 1 1 0 x x x	Not used	Not used	Not used	Not used	Not used
7 x x 1 1 1 x x x	Bias	Bias	Bias	Bias	Video mute

Note) After power on all TV outputs are off and muted.

Switch 2 (VCR Output) Data 3 Bits 3, 4, 5

Switch setting	Vout5 (Chroma (C))	Vout6 (CVBS/Y)	Comment
0 x x 0 0 0 x x x	VIN5	VIN8	Digital encoder
1 x x 0 0 1 x x x	VIN6	VIN9	Digital encoder
2 x x 0 1 0 x x x	VIN7	VIN10	VCR
3 x x 0 1 1 x x x	Not used	Not used	Not used
4 x x 1 0 0 x x x	VIN5	VIN3	Digital encoder
5 x x 1 0 1 x x x	Not used	VIN11	TV
6 x x 1 1 0 x x x	Not used	Not used	Not used
7 x x 1 1 1 x x x	Bias	Bias	Video mute

Note) After power on VCR outputs are off and muted.

VCR Chroma Mute Data 3 Bit 7

0 x x x x x x x = Vout5 active. Connected to input specified in above table.

1 x x x x x x x = Vout5 muted (the output dc bias still remains).

Standby Mode Control Data 6 Bits 0, 1, 2, 3, 4, 5

Each video output can individually be turned off using data byte 6.

0 = Video Output off

1 = Video Output on

Note) When switched off, the video outputs are high impedance to prevent d.c. driving of the external emitter follower stage.

The reduction of overall current consumption will depend on how many video outputs are turned off.

After power on all video outputs are in the off state.

4. Fast Blanking Operation (Pin 16 on SCART), FBLK

The fast blanking signal instructs the TV to select either the external CVBS information or the external RGB information. This is used to superimpose an on screen display (OSD) presentation (normally RGB) upon a CVBS background. Fast blanking information has the same nominal phase as the RGB and CVBS signal, and is defined as follows,

Fast blanking output at scart,

1. CVBS mode Scart pin voltage = 0 to 0.4V
2. RGB mode Scart pin voltage = 1 to 3.0V

Threshold voltage is approximately 0.75V at the scart input.

Fast Blanking I²C Control

In the CXA2126Q, there are two fast blanking inputs, one associated with the VCR RGB/CVBS input (FBLANK_IN2), and another associated with the Digital Encoder input (FBLANK_IN1). These can be selected by I²C. In addition to the two blanking inputs, the fast blank pin output can be set to a constant 0V or 5V by means of the I²C control. Hence there are four possible states. These are controlled according to the following table.

FBLK Control Data 5 Bits 3, 4, 5

I²C Setting	Fast Blank Output
0 x x 0 0 0 x x x	0V
1 x x 0 0 1 x x x	+5V
2 x x 0 1 0 x x x	Same level as Fast Blank in 1 (0/+5V)
3 x x 0 1 1 x x x	Same level as Fast Blank in 2 (0/+5V)
4 x x 1 0 0 x x x	Not used
5 x x 1 0 1 x x x	0V
6 x x 1 1 0 x x x	0V
7 x x 1 1 1 x x x	0V

Note) After power on the output is 0V.

Fast Blank output circuit

The output requires an external buffer stage to drive the required 75Ω scart termination.
The levels at the IC output are 0V and +5V.

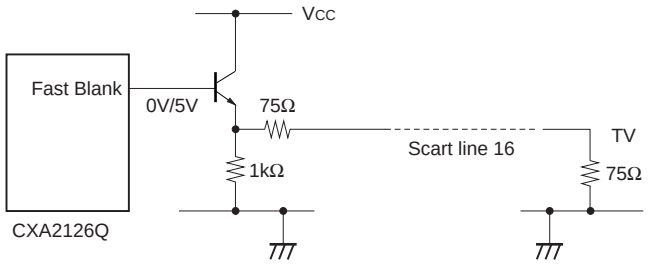


Fig. 4-1. Fast Blanking Interface to TV SCART

5. Function Switch, FNC.

The function switch facility is designed to read the status of the SCART function pin 8 from the VCR input. The read register holds the status of the input function line.

The function output is controlled by I^2C and is used to change the voltage on the function line to the TV. The output can be connected directly to the scart pin. (Fig. 5-1)

Read Mode

Reads the status of the input FNC_VCR.

Input Pin Voltage		Read Data8	
FNC_VCR	Level (SCART Defn.)	b1	b0
0 to +2V (default)	(Internal TV)	0	0
+4.5 to +7V	(16:9 External)	0	1
+9.5 to +12V	(4:3 External)	1	1

Write Mode

Controls the voltage at the TV function line (pin 8)

I^2C Control (Data 5)	Mode/(Typical pin Voltage)
0 x x x x x 0 0 x	Internal TV/(1V)
1 x x x x x 0 1 x	External scart input 16:9 mode/(6V)
2 x x x x x 1 0 x	External scart input 4:3 mode/(11V)
3 x x x x x 1 1 x	External scart input 4:3 mode/(11V)

Note) After power on output is internal TV mode ie. 0V at the pin.

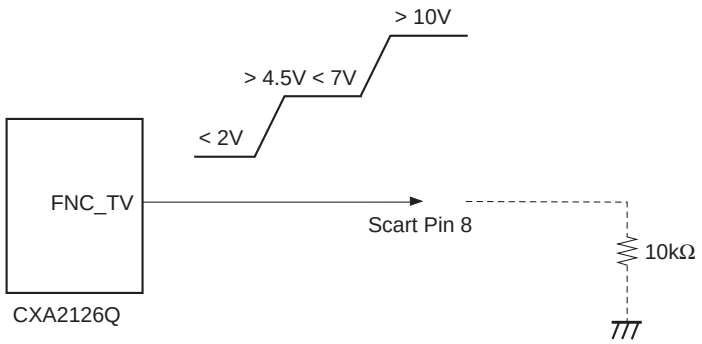


Fig. 5-1. TV Function Switch Output

6. Logic Output

A single logical output pin is provided. This is controlled via the I^2C and is an open collector output.

Specification

I^2C bit 0 = open collector/high output impedance

I^2C bit 1 = Vsat (to 0.2V)

Vmax at logic pin = 12V

Imax during current sink = 1mA

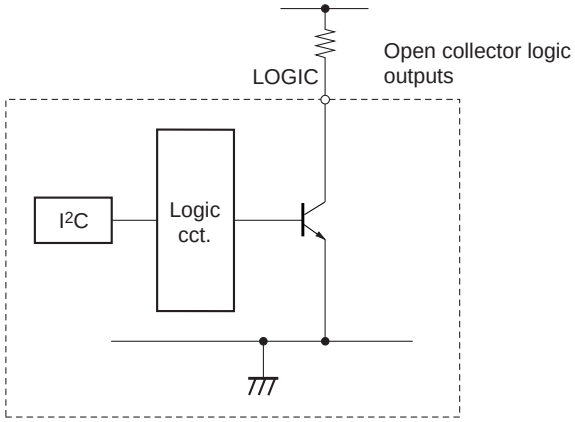


Fig. 6-1. Logic Output Interface

7. I²C Audio Signal Control

Outputs TV, VCR Data 2, 3 Bits 0, 1, 2

Switch Setting	RTV, ROUT1	LTV, LOUT1
0 x x x x x 0 0 0	Rin1	Lin1
1 x x x x x 0 0 1	Rin2	Lin2
2 x x x x x 0 1 0	Not used	Not used
3 x x x x x 0 1 1	Rin3	Lin3
4 x x x x x 1 0 0	Audio mute	Audio mute
5 x x x x x 1 0 1	Audio mute	Audio mute
6 x x x x x 1 1 0	Audio mute	Audio mute
7 x x x x x 1 1 1	Audio mute	Audio mute

Note) After power on the audio outputs are muted.

Volume Control Fine Data 1 Bits 2, 3, 4

Setting	Volume Fine Control Gain
0 x x x 0 0 0 x x	0dB
1 x x x 0 0 1 x x	–1dB
2 x x x 0 1 0 x x	–1dB
3 x x x 0 1 1 x x	–3dB
4 x x x 1 0 0 x x	–4dB
5 x x x 1 0 1 x x	–5dB
6 x x x 1 1 0 x x	–6dB
7 x x x 1 1 1 x x	–7dB

Volume Control Coarse Data 1 Bits 5, 6, 7

Setting	Gain
0 0 0 0 x x x x x	0dB
1 0 0 1 x x x x x	–8dB
2 0 1 0 x x x x x	–16dB
3 0 1 1 x x x x x	–24dB
4 1 0 0 x x x x x	–32dB
5 1 0 1 x x x x x	–40dB
6 1 1 0 x x x x x	–48dB
7 1 1 1 x x x x x	–56dB

TV output amplifier Data 7 Bit 6

x 0 x x x x x x = 0dB

x 1 x x x x x x = +6dB

Note) After power on the gain is set to 0dB.

TV Mono Switch Data 7 Bit 3

x x x x 0 x x x = Normal stereo output

x x x x 1 x x x = Mono signal switched onto R + L line.

VCR Mono Switch Data 7 Bit 4

x x x 0 x x x x = Normal stereo output

x x x 1 x x x x = Mono signal switched onto R + L line.

Mute and Zero Cross Operation

For TV, phono and mono outputs.

There are two mute control bits in the bus map to allow the TV outputs to be muted before the channel change instruction occurs. The normal structure for a click free audio channel change is as follows:

Data 1 Mute the TV audio output with the ZCD switched on

Data 2 Change the TV audio source.

Data 7 Un-mute the TV audio output again with the ZCD switched on.

TV Aud Mute Data 1 Bit 1 Data 7 Bit 7	**ZCD** Data 1 Bit 0	RTV, LTV, Phono_R, Phono_L, Mono outputs
0	0	Un-mute immediately
0	1	Un-mute on next zero cross
1	0	Mute immediately
1	1	Mute on next zero cross

Note) After power on TV mute and ZCD are set to 0.

Notes on operation

1) Supply de-coupling capacitors, 10nF and 4.7µF in parallel should be inserted as close to the supply pins, 20, 38, 60 as possible.

2) To minimize crosstalk, attention should be given to the routing of audio and video to the IC inputs. PCB track lengths should be kept as short as possible and preferably, audio placed on a separate layer to the video.

3) Attention should be given to the electrolytic capacitors on the input and output signal pins. As the pin's voltage is between 3.7V and 4.7V dc the positive terminal on the capacitor should be orientated towards the pin.

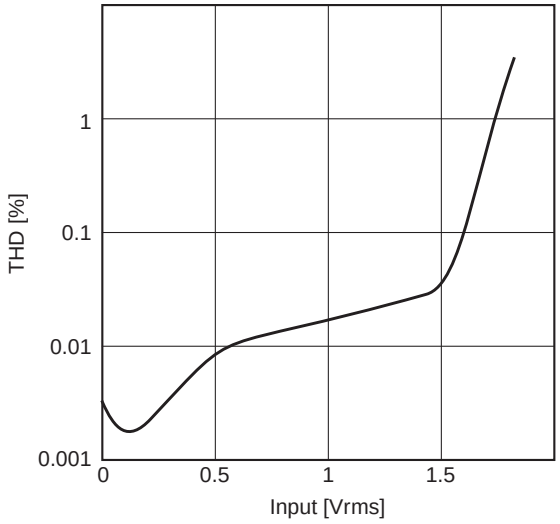
4) The audio outputs may be muted at any time after power up by connecting the HW_MUTE pin (45) to a voltage > 2.5V and < 9V.

5) When driving video loads with impedance = 75Ω an emitter follower or video line driver is required to be connected at the video outputs as shown in the application schematic.
   Stray capacitance on pins Vout1-8 must be kept to a minimum by placing loads as close to the pins as possible.

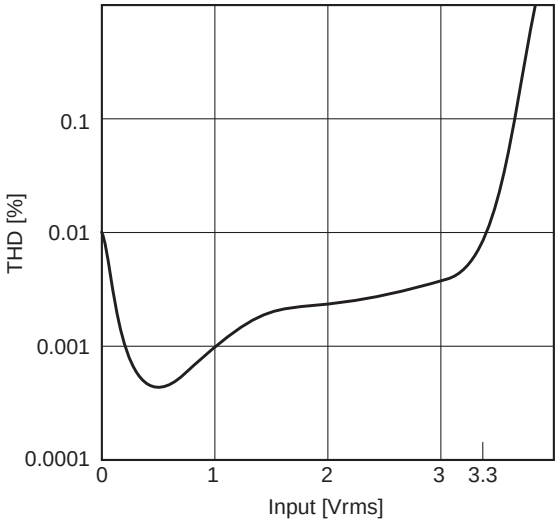
6) The supply voltage on pin 58 "V_{CC}_12V" should not exceed +12V. If the supply has poor regulation then a series diode or zener diode may be used to limit the voltage at this pin.

Typical audio output distortion

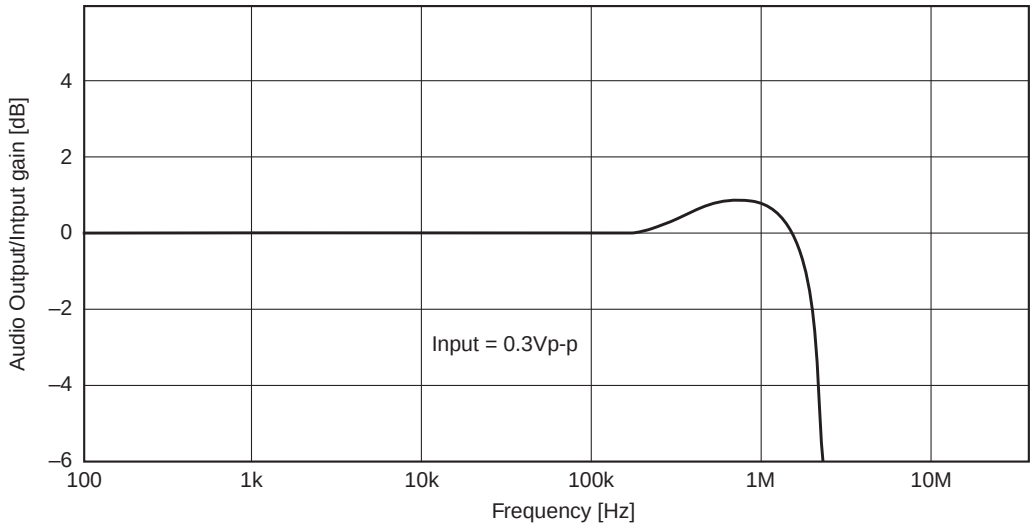
Inputs RIN1, LIN1 selected



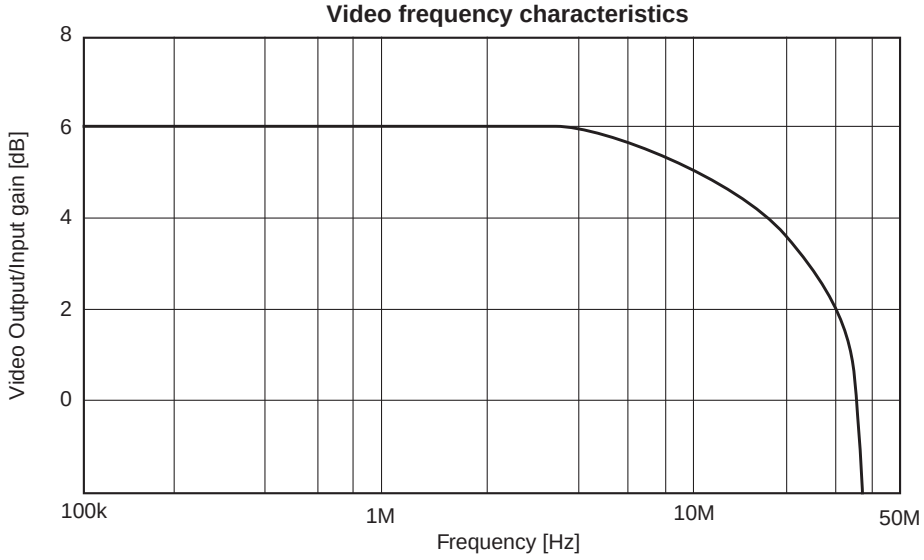
Inputs RIN2, 3/LIN2, 3 selected



Audio frequency characteristics

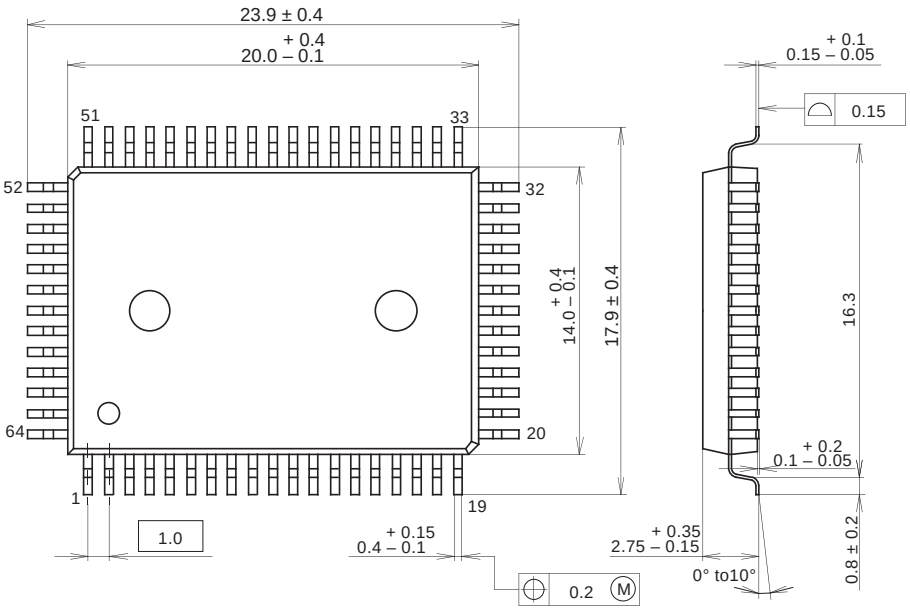


Video frequency characteristics



Package Outline Unit: mm

64PIN QFP(PLASTIC)



SONY CODE	QFP-64P-L01
EIAJ CODE	QFP064-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.5g